What Is Claimed Is:

Claim 1. A method for reducing power utilized by a processor comprising the steps of:

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determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled, and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disabled.

Claim 2. A method as claimed in Claim 1 in which the step of determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled comprising monitoring a stop clock signal.

Claim 3. A method as claimed in Claim 1 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled comprises furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor.

Claim 4. A method as claimed in Claim 3 in which the step of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled further comprises providing a feedback signal to the voltage regulator to reduce its output voltage below a specified output voltage.

Claim 5. A method as claimed in Claim 1 further comprising the steps of transferring operation of a voltage regulator furnishing core voltage in

a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled.

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Claim 6. A method as claimed in Claim 5 further comprising the steps of returning the voltage regulator to its original mode of operation when the lower value of the core voltage is reached.

Claim 7. A circuit for providing a regulated voltage to a processor comprising:

a voltage regulator having:

an output terminal providing a selectable voltage, and

an input terminal for receiving signals indicating the selectable voltage level;

means for providing signals at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in a computing mode.

Claim 8. A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises means for accepting binary signals indicating different levels of voltage.

Claim 9. A circuit as claimed in Claim 7 in which the means for providing signals at the input terminal of the voltage regulator comprises:

selection circuitry,

means for furnishing a plurality of signals at the input to the selection circuitry, and

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means for controlling the selection by the selection circuitry.

Claim 10. A circuit as claimed in Claim 9 in which:

the selection circuitry is a multiplexor, and

the means for controlling the selection by the selection circuitry includes a control terminal for receiving signals indicating a system clock to the processor is being terminated.

Claim 11. A circuit as claimed in Claim 7 further comprising means for reducing the selectable voltage below a level provided by the voltage regulator.

Claim 12. A circuit as claimed in Claim 11 in which the means for reducing the selectable voltage below a level provided by the voltage regulator comprises:

a voltage divider network joined between the output terminal and a voltage source furnishing a value higher than the selectable voltage, and

a voltage regulator feedback circuit receiving a value from the voltage divider network.

Claim 13. A circuit as claimed in Claim 7 further comprising:

circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases, and

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means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases.